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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/066,028 | 01/31/2002 | Peter T. Liu | 37310-000137 | 2099 |

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| EXAMINER |
|---|
| TRA, ANH QUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/066,028 | LIU, PETER T. | |
| | Examiner | Art Unit | |
| | Quan Tra | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17* is/are allowed.

6)☒ Claim(s) *2-5,7-13,15,16,18 and 20* is/are rejected.

7)☒ Claim(s) *6 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the amendment filed 03/18/04. the rejection in previous office action is maintained.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is misdescriptive and renders the claim indefinite. It is misdescriptive for reciting "the validation circuit dynamically adjusts a validation point based on the sense amplifier operating conditions…". It is seen in Applicant's figure 1 that the validation circuit is for indicating when the enable signal is applied. It is not seen the validation circuit is used to adjust any validation point.

Claims 9-13 are rejected as including the indefiniteness of claim 8.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2-5, 7-11, 13, 15,16, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoki (USP 6125069).

As to claim 18, Aoki's figure 15 shows a buried fuse reading device, comprising at least one buried fuse (the buried fuse in circuit 22 that located in the left), at least one sense amplifier (28, 32 in circuit 22 that located in the left) sensing a condition of the buried fuse; and a validation circuit (10, 28, 32, 17, 18 in circuit 22 that located in the right) mimicking, with a delay (10, 17, 18), the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid. (The output of inverter 18 in the left circuit 22 is low when signal FST is high regardless the state of the fuse in the right circuit 22. Thus, when the output of the inverter 18 is low, it is indicated that the output of the sense amplifier is valid).

As further called in for claim 8, insofar as understood, figure 15 shows the validation circuit dynamically adjust a validation point base on the sense amplifier operating conditions, the validation point being a point in time when the sense amplifier output is considered valid.

As to claim 2, figure 15 shows the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.

As to claim 3, 9 and 15, a circuit, not shown, that generating signal FST for powering the buried fuse reading device up and down; and wherein the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition once the power control circuit begins powering up the buried fuse reading device.

As to claims 4, 10, it is inherent for the circuit of figure 15 to have a bias generating circuit for generating first (Vdd) and second voltages (Vss); and wherein the sense amplifier operates based on the first and second voltages.

As to claims 5, 11, figure 15 shows the validation circuit operates based on the first and second voltages.

As to claims 7 and 13, Aoki's figure 15 further shows plurality of buried fuses (fuses 10 in the left and middle circuit 22); and a sense amplifier (28s, 32s, 24s) associated with each of the buried fuses.

As to claim 16, figure 15 shows the sense amplifier and the validation circuit draw substantially no current when the power control circuit (circuit that generating signal FST) has the buried fuse reading device power down.

As to claim 20, figure 15 shows the validation circuit is connected in parallel with the at least one sense amplifier and the at least one buried fuse.

***Allowable Subject Matter***

5. Claims 6 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 17 is allowed.

7. Claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 6 and 12 would be and claim 17 are allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a sense amplifier 50 includes first PMOS transistor (54) and a first NMOS transistor (56) connected in series with the buried metal fuse (52), a gate of the first PMOS transistor receiving the first voltage (BHI) and the gate of the first NMOS

transistor receiving the second voltage (BLO); the validation circuit (70) includes a second PMOS transistor (72) and a second NMOS transistor (74) connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistors, respectively.

Claim 19 would be allowable because the prior art fails to teach validation circuit is the same as the at least one sense amplifier except that the validation circuit includes weaker components.

***Response to Arguments***

8. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that Aoki fails to disclose a validation circuit mimicking, with a delay, the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid as recited in claim 18. The Examiner respectfully disagrees. The output of inverter 18 in the left circuit 22 is low when signal FST is high regardless the state of the fuse in the right circuit 22. Thus, when the output of the inverter 18 is low, it is indicated that the output of the sense amplifier is valid. Therefore, Aoki's figure 15 shows a validation circuit mimicking, with a delay, the sense amplifier regardless the state of the at least one buried fuse.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

May 24, 2004